D-MOT-10 FPGA IP CORE FOR MOTION DETECTION IN VIDEO STREAM IMAGES FPGA

The D-MOT-10 FPGA IP core for motion detection in video stream images is a completed module intended to be used in vision systems for various applications (security systems, specialized systems, etc.) that are based on FPGA. The core represents a simple data exchange interface that ensures easy integration into various systems. The algorithms are perfectly suitable for motion detection of ground, surface and aerial objects of any type.

The implemented algorithms provide detecting of small-size and low-contrast objects against a complex background. When an object is detected the core assigns it a unique number and determinates the movement direction. This makes it easy to track the object behavior and build efficient analytical system (perimeter defense, road traffic control and etc.) When a moving object is detected its motion path is calculated. In case the object disappears from the field of vision (for instance, behind an obstacle) the core predicts the path and detects the object when it re-appears. It is possible to detect up to 128 moving objects simultaneously. Thus, the D-MOT-10 IP core is a completed module that allows its use in any FPGA projects for vision systems.

BASIC CHARACTERISTICS

Max *number of moving objects detecting simultaneously is up to* ***128****.*

Max *size of detecting object is limited by the size of processed area.*

Min *size of detecting object is* ***8x8*** *pixels size in an image area.*

Max *speed of the object for its stable detection is no more than* ***30*** *pixels per frame.* ***Min*** *speed no less than* ***0.1*** *pixels per frame in any direction.*

Stable detection of moving objects with contrast from ***10%****.*

Max *frame size is up to* ***720x576*** *pixels. When it is needed to process big images it is recommended to use several cores simultaneously.*

Output coordinates are obtained with ***1*** *pixel accuracy.*

Output coordinates delay is ***1*** *frame.*

Processing of grayscale images with the bitness of ***8 bits/pixel****.*

Output information on the detected objects is ***detecting strobe position****, its unique* ***number*** *and* ***motion direction****.*

INTERACTION INTERFACE

The figure shows the interaction of the IP core with FPGA project.

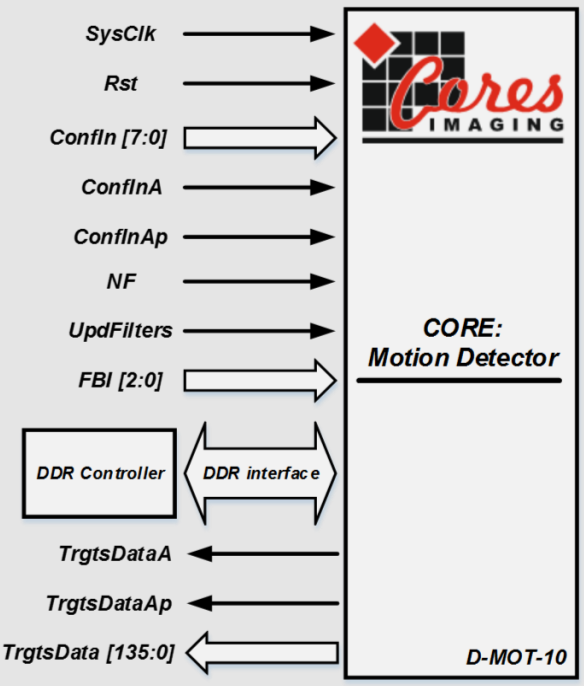
SysClk *— Clock signal for the core. All signals for the core must be synchronized with SysClk.*

Rst *— Core reset signal.*

ConfIn[7:0], ConfInA, ConfInAp *— Interface for writing configuration registers.*

NF *— New frame signal.*

UpdFilters *— The core filters reset signal.*



FBI[2:0] *— Bus for the current frame buffer index.*

DDR interface *— Unified interface for data exchange with the DDR Xilinx®.*

TrgtsData[135:0], TrgtsDataA, TrgtsDataAp *— Interface for the output of information about the coordinates of detected objects.*

The configuring of the core (writing of the configuration registers) is carried out before the work is started. Moreover, the writing of the configuration registers can be performed during the core operation if necessary. The core gives for each of the detected objects the coordinates of the detecting strobe corners, its unique number and motion direction as speed components in screen coordinates.

More detailed information on the interaction interface can be found in the document Programmer_Manual.

WORKING PRINCIPLE

The core is connected to the interface controller of DDR memory via a standard interface (controller provided by Xilinx Company) from which it reads the current images of video sequence and where it writes the results. The designer should ensure refreshment of image frames in the DDR memory according to multi-buffer principle (multiple buffering). Before operation is started, the core should be configured (configuration register values need to be written). Observed scene (the scene in the images of the video sequence) should be fixed. After initialization the core (core switching) it needs some time (2-3 minutes) to adapt to the observed scene. During this time, the core algorithms initialize filters and form the map of constantly moving objects (e.g. treetops wave in the wind). During this time false detections are possible. After all core filters are adapted all moving objects are detected with the high degree of reliability. Herein only objects having a specific trajectory (not accidental movement in an image frame) are detected. When a moving object is detected the core algorithms estimate its size and assign to it a unique numerical code that can be used in the further processing outside the core. The core gives the information about moving objects for each frame in the video sequence. For each detected moving object the core gives the coordinates of the corners of the detecting strobe in the image plane, numerical number assigned to the object, as well as its movement direction, all of that allows to build effective perimeter control and traffic analysis systems on the basis of the core.

SUPPORTED PLATFORMS

The core can be used in any vision applications such as security video surveillance systems and in special robotic vision systems. A simple interface of data exchange with the core makes it possible to integrate it easily into any FPGA project. The D-MOT-10 IP Core is synthesized for the platforms of ***Xilinx®*** *Company and is available by request with* ***FPGA Xilinx®*** *type specified.*

The core is transferred to the customer in a synthesized form for a particular type of FPGA license.

The following families of FPGA by Xilinx ® are supported:

Artix-7, Artix-7Q, Kintex-7, Kintex-7Q, Virtex-7, Virtex-7Q, EasyPath-7, Virtex-6, Virtex-6Q, EasyPath-6, Spartan-6, Virtex-5Q, Virtex-5QV, Virtex-4Q, Virtex-4QV, XA Spartan-6, XA Spartan-3A, XA Spartan-3A DSP, XA Spartan-3E.

REQUIRED RESOURCES

The following table contains the resources required for the T-COR-10 IP Core for certain types of ***FPGA Xilinx®****.*

FPGA Type	Slice Registers	DSP	Block Memory
Artix-7 XC7A100T-3	5114 (4%)	11 (4%)	40 (29%)
Kintex-7 XC7K410T-2L	5113 (<1%)	11 (1%)	40 (5%)
Virtex-7 XC7VX330T-2L	5113 (<1%)	11 (<1%)	40 (5%)
Virtex-7 XC7V2000T-2L	5113 (<1%)	11 (<1%)	40 (3%)
Virtex-6 XC6VLX240T-2	5116 (1%)	11 (1%)	40 (9%)
Spartan-6 XC6SLX150T-3	5206 (2%)	13 (7%)	31 (11%)
Zenq-7 XC7Z045-2	5113 (<1%)	11 (<1%)	40 (7%)

Note: The data may vary according to the particular project characteristics.

CONTACTS

Scientific and Production Company RIFTEK is an enterprise specializing in development and fabrication of optoelectronic instruments for measuring of geometrical quantities.

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Cores IMAGING