S-COR-10 IMAGE STABILITHATION IP CORE

Programmer manual

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CONTENTS

INTRODUCTION 3
CORE VERSIONS 3
BASIC CHARACTERISTICS 3
DESCRIPTION AND OPERATION PRINCIPLE 3
APPLICATION FIELD AND PLATFORMS USED 4
PROCEDURE OF USE 4
PERFOMANCE 4
REQUIRED RESOURCES 5
REQUIREMENTS FOR FGPA PROJECT 5
DESCRIPTION OF INTERFACE 5
CONFIGURING THE CORE 6
OUTPUT INFORMATION 6
CONNECTING THE CORE TO FPGA PROJECT 6
CONTACTS 7

INTRODUCTION

The S-COR-10 FPGA IP core for image stabilization in video stream images is designed for use in vision systems intended for various applications (security systems, specialized systems, etc.) that are based on FPGA. The core is a completed module suitable for use in FPGA projects. The core represents a simple data exchange interface that ensures easy integration into various systems. The core performs 2D (horizontal and vertical) image stabilization. The algorithms implemented in the core provide image stabilization with accuracy of 2 pixels. The core determines the offset of the image relative to the previous frame and adapted to the smooth movement of the field of view of the video source. The core doesn't modify the input image, the core forwards horizontal and vertical offset values to other subsystems. Subsequently this information can be used to read image data from the corresponding addresses (with offset). Thus, the S-COR-10 IP core is a versatile module that allows its use in any FPGA projects for vision systems.

CORE VERSIONS

Versions of the S-COR-10 IP core are shown in Table 1.

Table 1 – Versions of the S-COR-10 IP core.

Version	Notes
1.0	First version of the IP core. Implements a high-performance correlation algorithm for image stabilization.

BASIC CHARACTERISTICS

The S-COR-10 IP core ensures calculations for image stabilization. The basic characteristics of the core are given in Table 2.

Table 2 – Basic characteristics of the S-COR-10 IP core.

Parameter	Values and notes
Max video frame size	1024x1024 pixels.
Min video frame size	128x128 pixels.
Offset determination accuracy	2 pixels for a single offset
Maximum offset of the current frame relatively to previous	32 pixels in any direction
Calculation time	No more than 3 ms. when for frame size 720x576 and no more than 10 ms. for frame size 1024x1024. The system frequency is 200 MHz.
Input information requirements	In the images no more than 20% of contrast moving objects, no less than 20% of contrast stationary background objects.

Note: the data above is given for FPGA Kintex-7.

DESCRIPTION AND OPERATION PRINCIPLE

The core is a complete module intended for use in FPGA system vision projects. The core works as follows. Video streaming enters the core (regular video frames). The core receives video information and stores it into internal memory after preprocessing. After the next frame is received the core calculates the offset of a current frame relative to the previous one. After the offset is calculated, the core processes obtained offset values to compensate smooth displacement of the field of view of the video source. The processed coordinates of the frame offset are forwarded to the consumer via an output interface.

APPLICATION FIELD AND PLATFORMS USED

The core can be used in any vision applications such as security video surveillance systems and in special robotic vision systems. A simple interface of data exchange with the core makes it possible to integrate it easily into any FPGA project. The core is made available to customer with specification of FPGA type. The core is delivered to the customer in a synthesized form for a specific type of FPGA under license. The core was developed for FPGA's of Xilinx Company and supports the following of their families:

Artix-7, Artix-7Q;
Zenq-7, Zenq-7Q;
Kintex-7, Kintex-7Q;
Virtex-7, Virtex-7Q;
Virtex-6, Virtex-6Q;
Spartan-6;
Virtex-5Q, Virtex-5QV;
Virtex-4Q, Virtex-4QV.

PROCEDURE OF USE

The use of the S-COR-10 IP core the designer should provide the format required and the procedure of transmission video stream data to the core. Being started the core must be configured. Configuring the core means recording the values of width and height of the processed video frames. Once the core received the configuration data (width and height of video frames), the transfer of video data can be started. Video data is transmitted continuously as data exchange interface is described and upon receipt from the video source. The core itself selects the necessary data and performs processing. The core gives the offset data upon processing and no later than time intervals after receiving the next video frame stated in the characteristics. The detailed description of the core usage is given below.

PERFOMANCE

The IP core characteristics given in Table 2 have been calculated from the results of tests performed on FPGA Xilinx Kintex-7. The performance characteristics depend significantly on the type of FPGA and image refresh rate. Table 3 shows throughput characteristics of the core and their specific features.

Table 3 – Basic characteristics of the S-COR-10 IP core and their specific features.

Parameter	Values and notes
Maximum size of processed frames	The core is capable to process frames up to 1024x1024 pixels. To use the core with one or another frame resolution, it should be configured in an appropriate way at the start.
Minimum size of processed frames	Minimum size of video frames is 128x128 pixels. Frame resolution lower than stated leads to incorrect operation of the core.
Offset measurement accuracy	Horizontal and vertical output data offset accuracy is equal to 2 pixels for a single offset. In case of continuous offset of the field of view of the video source output information is compensated according to the displacement and output coordinates accuracy may be lower in the direction of smooth movement of the field of view of the video source.
Maximum offset of the current frame relative to the previous one	32 pixels per frame in any direction. Displacement of the current image relative to the previous by more than 32 pixels leads to incorrect operation of the core.
Calculation time	No more than 3 ms. when for frame size 720x576 and no more than 10 ms. for frame size 1024x1024. The system frequency is 200 MHz. At a lower system frecuency calculation time increases proportionally to the decrease of the project frequency

Parameter	Values and notes
	(clock frequency).
Input information requirements	In the images no more than 20% of contrast moving objects, no less than 30% of contrast stationary background objects. Contrast objects are considered objects in which the contrast of digital images in video frame is more than 15%.

Note: the data above is given for FPGA Xilinx Kintes-7.

REQUIRED RESOURCES

Table 4 shows the resources required for the S-COR-10 IP core for various FPGA's of Xilinx company.

Table 4 – Resources required for the S-COR-10 IP core.

FPGA chip	Slice Rigisters	Slice LUTs	BRAM
Kintex-7 xc7k325t-2ffg676	2068/407600 (<1%)	2834/203800 (1.3%)	112/445 (25.1%)
Artix-7 xc7a100t-2fgg676	2068/126800 (1.8%)	2831/53400 (5.3%)	112/135 (82.9%)
Virtex-7 xc7vx330t-2ffg1157	2068/408000 (<1%)	2834/204000 (1.3%)	112/750 (14%)

REQUIREMENTS FOR FGPA PROJECT

Special requirements for the organization of FPGA project are not requested. The designer should observe the core configuration sequence. The core should be recorded according to the description of the interface. Configuration data transfer and receiving the data from the core is carried out via UART standard interface.

DESCRIPTION OF INTERFACE

Figure 1 shows the interface for interaction with the S-COR-10 IP core.

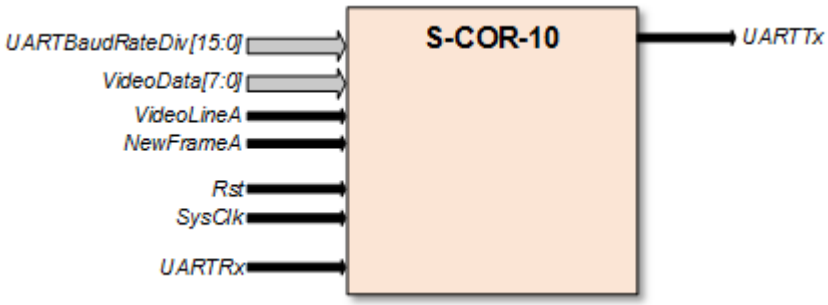

Figure 1 – Interface for interaction with the S-COR-10 IP Core

All input and output assignments are given in Table 5.

Table 5 – Input and output assignments of the S-COR-10 IP core.

Name of signal	Assignment and notes
SysClk	Clock signal for the core. All signals for the core (control, configuration, configuration, reset, etc.) must be synchronized with SysClk.
Rst	Core reset signal. The signal must be synchronous with SysClk and have a duration of 1 clock cycle. The reset signal is used 1 time at the beginning of work of the core before the configuration data transfer.
UARTRx	*UART* to transfer configuration data to the core.
UARTBoundRateDiv[15:0]	Frequency divider for SysClk UARTRx and UARTTx.
VideoData[7:0]	Video data. 1 byte of data per 1 clock cycle (1 SysClk). Video

Name of signal	Assignment and notes
	data should be transmitted in the format of 8 bit per pixel (mono_8). Video data should be transmitted via image lines (lines should go sequentially). This means the data is transmitted continuously for each image line.
VideoLineA	Data line strobe.
NewFrameA	New frame start signal. NewFrameA signal duration should be equal to 1 clock signal SysClk. At this signal the core starts
UARTTx	*UART* to transfer output data from the core.

All the data exchange interfaces are synchronized to *SysClk* signal. Figure 2 shows the timing diagrams for the exchange of data via S-COR-10 interfaces.

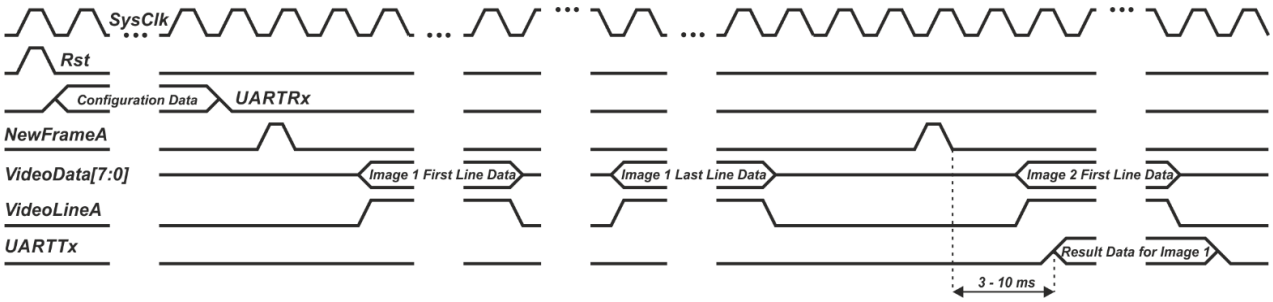

Figure 2 – Timing diagrams for the exchange of data via S-COR-10 interfaces

CONFIGURING THE CORE

Before the work is started, the S-COR-10 IP core should be configured. Configuring consists in writing of the configuration registers via the interface UARTRx after the reset signal Rst. Configuration data includes width and height of the processed image. Table 6 shows the format of configuration data.

Table 6 – Parameters of the IP core available for setting.

Byte №	0	1	2	3
Value	W high byte	W low byte	H high byte	H low byte

W – width of the processed image. Format: unsigned short int;
H – height of the processed image. Format: unsigned short int.

OUTPUT INFORMATION

The information from the IP core S-COR-10 is available via the line UARTTx. Output data format is shown in Table 7.

Table 7 – Output data format.

Byte №	0	1	2	3	4	5
Value	W high byte	W low byte	H high byte	H low byte	dX	dY

W – width of the processed image. Format: unsigned short int;
H – height of the processed image. Format: unsigned short int;
dX – horizontal frame offset. Format: signed char;
dY – vertical frame offset. Format: signed char.
Image offset direction corresponds to the window coordinate system (coordinate starts in the left upper corner).

CONNECTING THE CORE TO FPGA PROJECT

Since the core is supplied for the FPGA Xilinx project, the procedure of connection of the S-COR-10 IP core is presented for IDEISE 14.7. The core represents a file with extension *. ngc and a file with extension *.v (On request, we can supply *. Vhdl) (S_COR_10.ngc, S_COR_10.v (.

Vhdl)). The file S_COR_10.ngc is the synthesized core. The file S_COR_10.v (. Vhdl) is the shell where the core inputs and outputs are specified. Below is the procedure of using the core in an FPGA project with a HDL upper level in IDE Xilinx ISE 14.7.

1. Copy the file S_COR_10.v (.vhdl) to your project folder.
2. Add the file S_COR_10.v (.vhdl) to the project.
3. Place a copy of the core in the high module.
4. Connect the inputs and outputs of the core with the infrastructure of the project.
5. In the project synthesis parameter «Cores Search Directories» specify the path to the file S_COR_10.ngc.

After resetting the module, it is configured to work with the image size 720x576 (default) pixels and can be used immediately. If it is needed to work with images of other dimensions, the core should be configured via UART interface after resetting according to the protocol given in «CONFIGURING THE CORE» section.

Frame buffer controller module BRAMFrameController.v with the file Xilinx CoreGen FrameBRAM.xco. is supplied with the core to speed up integration of the core in ready projects. FrameBRAM.xco file comes as a sample of frame memory based on the block memory FPGA.

CONTACTS

RIFTEK – a private company dealing with development and production of optoelectronic devices intended for measuring geometric quantities and video processing tools.

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