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SENSORS & INSTRUMENTS

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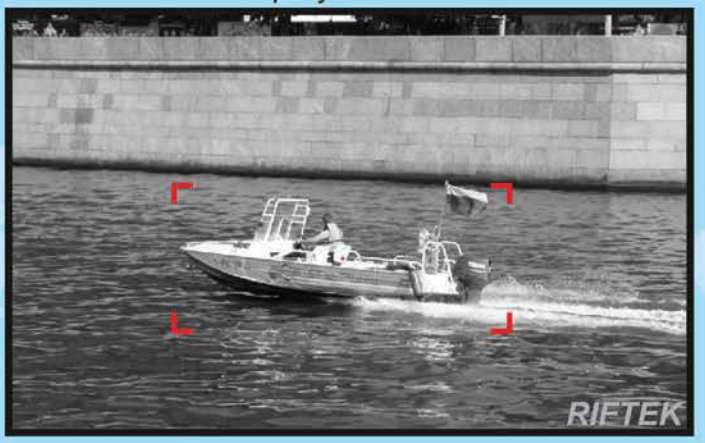
from RIFTEK Cores IMAGING

Video Tracking and Image Processing Cores

T-COR-10 FPGA IP Core for tracking objects in video stream images

Intellectuals Property object tracking cores (IP cores) supplied by RIFTEK ensure stable tracking of various classes of objects such as vehicles, flying objects, surface objects and humans. The IP cores are capable of operation with any video sources featuring resolution up to 2048x2048 pixels. Video source for IP cores can be provided by both common cameras and thermal vision cameras. The IP cores allow simultaneous tracking of several objects. A simple data exchange interface ensures easy integration of the IP cores into any FPGA-base technical vision systems. The cores require a little use of FPGA resources, which allows one to combine several cores in one project. Our IP cores support all FPGA families of Xilinx company.

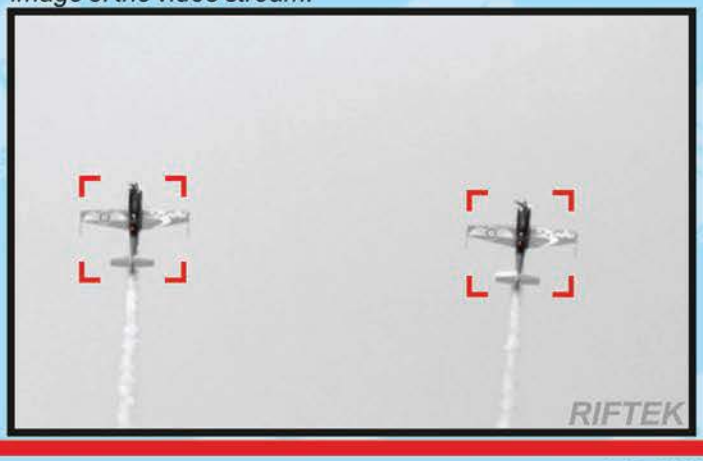


*The **T-COR-10 FPGA IP core** supports tracking of up to 5 objects in images of video sequence at the frame refresh rate of up to 30 Hz. User carries out capture of object for tracking and aborts object tracking. User can control the size and position of the tracking strobes. As output information the core gives the position of tracking objects in the image in the screen coordinate system. The core makes it possible to track small-size and low-contrast objects moving at various speeds against a complex background. The core implements unique highly efficient algorithms of tracking that allow their use in tackling any problems. The core represents a simple and effective interaction interface. It can be easily used in any FPGA projects. The designer using the core does not have a need for any special organization of an FPGA project.*

All interfaces used in the core are standardized. The IP core interacts with DDR memory controller directly. The designer has only to link the interfaces used. Control of the core operation modes is organized through a simple unified interface. Initial configuration of the core is effected via a configuration-register-write interface (analogous to control interface). The data output interface is also similar to the control interface. A simple data exchange interface allows easy transfer of the core from one project to the other.

OPERATION PRINCIPLE

The core ensures detection of coordinates of up to 5 objects in video stream images. Position of tracking object is determined in the screen coordinate system. Capture of objects for tracking and rejection of tracking is performed by a command transmitted via of a special interface. The core reads the next frame from the DDR memory and performs its processing. The output information is presented as position of tracked objects in each processed image of the video stream.



BASIC CHARACTERISTIC

Tracking mode: *correlational.*

Maximum number of tracking objects: *the core ensures tracking of up to 5 objects at strobe size of 40x40 pixels and frame refresh rate of 25 Hz.*

Maximum and minimum sizes of the tracking strobe: *the maximum strobe size at capture and tracking is 128x128 pixels. The minimum size is 8x8 pixels. The size of the tracking strobes can be changed independently for each object under tracking by commands as well as in the course of tracking.*

Maximum movement speed of tracking objects: *With a sudden change of the object position - no more than 15 pixels per frame. With a steady motion of the object, the speed is limited by the capability of the tracker system used.*

Minimum size of tracking object: *the core ensures stable tracking of objects of up to 3x3 pixels size.*

Minimum contrast of tracking objects: *stable tracking is achieved at a minimum contrast of the tracking objects against a uniform background of not less tan 10%.*

Maximum size of frames in video sequence: *The core operates with frames of up to 2048x2048 pixels size.*

Elongation of tracking objects: *tracking objects can have any configuration within the maximum size range of tracking strobes.*

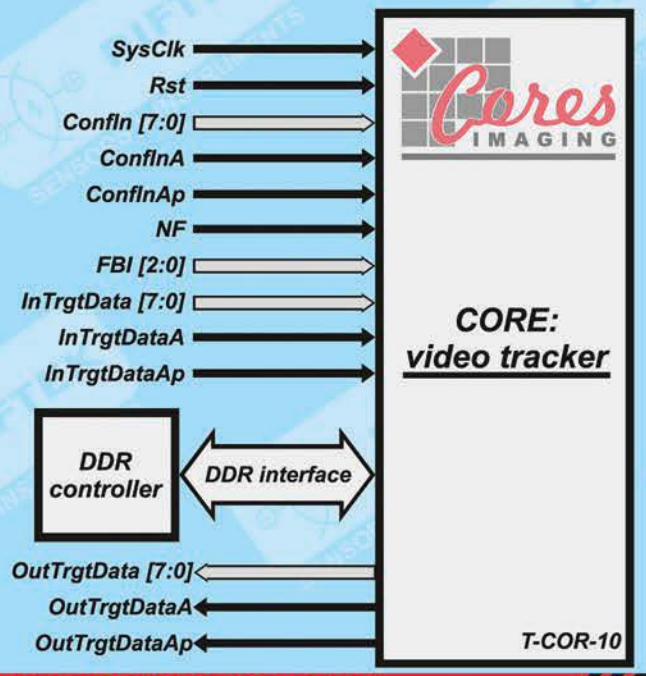
Tracking accuracy: *the output coordinates of tracking objects are obtained at an accuracy of 1 pixel.*

Time lag of output coordinates: *at the frame refresh rate of 25 Hz and recommended sizes of the tracking strobe, the core calculates the object coordinates before the end of the next frame in the video sequence (delay is 1 frame).*

Format of processed images: *the core works with images having color palette of 256 colors (grayscale) – 8 bits/pixel.*

The core throughput characteristics and the number of tracking objects can depending on FPGA type used. The characteristics presented here are based on testing of FPGASpartan-6 150. More detailed technical data of the core are given the Programmer Manual.

The figure shows the scheme of the IP core interface.



DATA EXCHANGE INTERFACE

The data exchange interface e is shown in the figure. Assignments of the lines are as follows:

SysClk *- clock signal (frequency depends on FPGA type);*

Rs t *– core reset signal;*

ConfIn[7:0], ***ConfInA***, ***ConfinAp*** *– configuration-register-writing interface;*

NF *- signal of new frame arrival for reading from the memory;*

FBI[3:0] *- Bus for the index of memory space from where the current image frame must be read;*

InTrgtData[7:0], ***InTrgtDataA***, ***InTrgtDataAp*** *- control data transmission interface;*

DDR interface *– unified interface for data exchange with DDR memory controller;*

OutTrgtData[7:0], ***OutTrgtDataA***, ***OutTrgtDataAp*** *– tracked object data output interface. A detail description of the interface for interaction with the core is given in the core datasheet.*

FPGA FAMILIES SUPORTED BY THE IP CORE

The core was developed for FPGA's of Xilinx company and supports the following of their families:: Artix-7, Artix-7Q, Kintex-7, Kintex-7Q, Virtex-7, Virtex-7Q, EasyPath-7, Virtex-6, Virtex-6Q, EasyPath-6, Spartan-6, EasyPath, VirtexSQ, VirtexSQV, Virtex-4Q, Virtex-4QV, XA Span:an-6, XA Spartan-3A, XA Spartan-3A DSP,XASpanan-3E.

REQUIRED RESOURCES

The following resources are required for the implementation of the FPGA Xilinx Spartan-6 XC6SLX150T-3 project:
Slice: 4133 (20%)
DSP48A1S:37(21%)
Block memory: 112 (42%).
For other FPGA types, the resources required can be different.
The core throughput characteristic is also dependent on the FPGA type used, clock frequency and operation mode. More detailed technical specifications of the core are given the Programmer Manual.

For additional information and purchasing please write to info@riftek.com.

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